## AMENDMENTS TO CLAIMS

Please cancel claims 1-8. Please add new claims 9-16.

Claims 1-8 (Cancelled)

9. (New) A field programmable gate array (FPGA) comprising:

a gate array;

at least one programmable voltage supply driver coupled to the gate array and configured to supply a plurality of voltages; (5)

a plurality of programmable input / output buffers coupled to the voltage supply driver and configurable to separate the voltage supplies; (page 2)

at least one fuse address driver coupled to the plurality of programmable input / output buffers and configured to drive the plurality of programmable input / output buffers; and

means to program the plurality of programmable input / output buffers to a desired configuration.

10. (New) The FPGA of claim 9, each of the plurality of programmable input /output buffers further comprising:

at least 2 programmable antifuse matrix cells configured to receive configuration information for the each of the plurality of programmable input / output buffers.

11. (New) The FPGA of claim 9, each of the plurality of programmable input /output buffers further comprising:

a set of programmable antifuse matrix cells configured to receive configuration information for the each of the plurality of programmable input / output buffers.

12. (New) The FPGA of claim 11, where each set of programmable antifuse matrix cells further includes 16 programmable antifuse matrix cells.

13. (New) The FPGA of claim 12, wherein the at least one fuse address driver further comprises a plurality of fuse address drivers and the at least one programmable voltage supply driver further comprises a plurality of programmable voltage supply drivers, wherein each set of programmable antifuse matrix cells is connected to eight of the plurality of fuse address drivers and two of the plurality of programmable voltage supply drivers.

14. (New) The FPGA of claim 9, further comprising:

a programmable input / output driver circuit coupled to the plurality of programmable input / output buffers, wherein the plurality of programmable input / output buffers further comprise a plurality of programmable antifuse matrix cells.

15. (New) The FPGA of claim 9, where said means to program further includes a plurality of programmable antifuse matrix cells.

16. (New) The FPGA of claim 9, where said desired configuration includes a plurality of I/O standards.